PATENT
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FM DEMODULATOR FOR A LOW IF RECEIVER

Related Applications:

This application claims priority under 35 U.S.C. § 119(e) of the co-pending U.S. provisional application Serial Number 60/167,196 filed on November, 23,1999 and entitled "FM DEMODULATOR FOR A LOW IF RECEIVER." The provisional application Serial Number 60/167,196 filed on November, 23,1999 and entitled "FM DEMODULATOR FOR A LOW IF RECEIVER" is also hereby incorporated by reference.

Field of the Invention:

This invention relates to the field of receivers. More particularly, this invention relates to a method of and apparatus for demodulating an FM signal using a low IF receiver.

Background of the Invention:

In a superhet receiver, also known as a superheterodyne receiver, an incoming modulated RF (radio-frequency) carrier signal is converted to an IF (intermediate-frequency) carrier value for additional amplification and selectivity prior to demodulation. Often, a superhet receiver is coupled with a pulse count FM (frequency modulation) or FSK (frequency shift keying) demodulator for recovering a desired audio-frequency signal.

Standard techniques for designing a superhet receiver with a pulse count demodulator include the use of hard limiting amplifiers instead of linear IF amplifiers and AGC (automatic gain control) schemes to minimize the design complexity. Such a technique is well known for FM or FSK receivers using a higher IF frequency.

Figure 1 illustrates a block diagram of a conventional radio IF and demodulator with a moderately low IF and pulse counting demodulator. A modulated RF input is received by an amplifier 10. An output of the amplifier 10 is coupled to a mixer 20. The mixer 20 is coupled to provide its output to an IF filter 40. The modulated RF signal is combined with a local oscillator signal to produce a modulated IF signal as output of the IF filter 40. The IF signal is comprised

of a modulated signal, which is the signal the receiver is designed to recover, and the carrier signal. The frequency of the carrier signal is the IF frequency. The combination of the amplifier 10, the mixer 20 and the IF filter 40 is conventionally referred to as a superhet receiver. The IF filter 40 is coupled to an IF limiter 50 via some means of ac coupling. The IF limiter 50 receives the IF signal, removes the amplitude information from the IF signal and outputs a square wave IF signal. The remaining characteristics of the square wave IF signal are the same as the IF signal input into the IF limiter 50.

The frequency modulation is found in the period of the output pulses of the IF limiter 50. This "pulse count demodulator" function is also known as a "frequency to voltage converter." The pulse count demodulator comprises a monostable 60 and a data filter 70. The IF limiter 50 is coupled to the monostable 60. The monostable 60 is triggered once for every cycle at the IF frequency. In other words, the monostable 60 will generate one output pulse for each cycle at the IF frequency. The output of the monostable 60 has a strong component at the carrier signal IF frequency and a weaker component at the modulated signal modulating frequency. The resulting output signal spectrum is dominated by the IF frequency whereby the mean rate pulse of the monostable 60 is the same as the IF frequency.

The output pulses of the monostable 60 are received by the data filter 70. The data filter 70 filters out the IF frequency components and passes the modulation frequency components thereby recovering the desired audio frequency signal. When designing the data filter 70, compromises must be made to take into account the following: the lower the IF frequency the stronger the recovered modulation component but the lower the IF frequency the less the difference between the modulation component and the IF frequency. A realizable data filter needs to remove the IF frequency while passing the modulation frequency.

A known limitation of the technique described in relation to Figure 1 is that the output of the monostable contains more unwanted energy at the IF frequency than wanted energy at the modulation frequency. In other words, the output from the monostable is dominated by the IF frequency which makes the process of filtering out the IF frequency while passing the

modulation frequency much more difficult. For proper filtering to occur, the IF frequency must be at least twice the bit rate of the transmission. For example, with a bit rate of 1 Mbits per second, the IF frequency must be at least 2 MHz. Many applications exist that require the use of a lower IF frequency, often a frequency which is of the same order or lower than the bit rate of transmission.

What is needed is a superhet receiver and demodulator circuit which is capable of recovering FM or FSK modulation from a lower IF frequency, an IF frequency which is often of the same order or lower than the bit rate of transmission.

Summary of the Invention:

A superhet receiver with quadrature IF and improved demodulator is configured to recover a modulated signal from a low IF in a radio receiver. A superhet receiver receives a FM radio-frequency signal, converts the input RF signal to an in-phase IF signal and an IF signal in phase quadrature to the in-phase signal, and outputs the IF signals. A plurality of monostables receive the IF signals and each monostable generates a corresponding output pulse. By combining the monostable output pulses, a complex waveform is generated. The complex waveform includes the modulated signal at the low IF and a carrier signal at a significantly higher IF. The complex waveform is filtered to recover the desired modulated signal.

Brief Description of the Drawings:

Figure 1 illustrates a block diagram of a superhet receiver with a pulse count demodulator of the prior art.

Figure 2 illustrates a block diagram of the preferred embodiment of the present invention.

Figure 3 illustrates an example of digital data to be transmitted via a FM radio-frequency signal and received by the present invention.

Figure 4 illustrates the in-phase and quadrature IF filter output signals in response to the input FM radio-frequency signal which carries the digital data illustrated in Figure 3.

Figure 5 illustrates the monostable output pulses in response to the in-phase and quadrature IF filter output signals of Figure 4.

Figure 6 illustrates the demodulator output in response to the monostable output pulses of Figure 5.

Detailed Description of a Preferred Embodiment:

A block diagram of a superhet receiver with quadrature IF and improved demodulator of the preferred embodiment of the present invention is illustrated in Figure 2. An amplifier 100 receives a FM radio frequency (RF) signal. The RF signal has an instantaneous frequency which varies above and below the nominal frequency based on the modulation. The amplifier 100 is coupled to an I-channel mixer 102 and a Q-channel mixer 104. The amplifier 100 increases the RF signal level to overcome noise in the mixers 102 and 104.

The I-channel mixer 102 combines the modulated RF signal from the amplifier 100 with a local RF oscillator signal to produce a modulated intermediate-frequency (IF) signal as output. The difference in frequency between the modulated RF signal and the local RF oscillator frequency is small, preferably in the order of 1 MHz. When the I-channel mixer 102 combines the modulated RF signal and the local RF oscillator signal, two signals are initially generated. The first signal is a sum of the local RF oscillator signal and the modulated RF signal, the sum is approximately two times the modulated RF signal since the frequencies of the local oscillator and modulated signals are nearly equal. This first signal is filtered away immediately. The second signal is a difference between the local RF oscillator signal and the modulated RF signal, which results in a low IF frequency in the order of 1 MHz. The low IF signal is the signal that is output from the I-channel mixer 102.

The Q-channel mixer 104 combines the modulated RF signal from the amplifier 100 with a local phase-shifted RF oscillator signal to produce a phase-shifted IF signal as output. The local phase-shifted RF oscillator signal is in phase quadrature with the local RF oscillator signal. In other words, the two signals are shifted 90 degrees apart. Specifically, the preferred

embodiment provides for the local RF oscillator signal to lead the local phase-quadrature RF oscillator signal by 90 degrees. As with the I-channel mixer 102, there are two signals produced when the Q-channel mixer 104 combines the modulated RF signal and the local phase-quadrature RF oscillator signal. The first signal is a sum of the local phase-quadrature RF oscillator signal and the modulated RF signal, which is approximately two times the modulated RF signal since the frequencies of the local phase-quadrature oscillator and the modulated signals are nearly equal. This first signal is filtered away. The second signal is a difference between the local phase-quadrature RF oscillator signal and the modulated RF signal, which results in a low IF frequency in the order of 1 MHz. The second low IF signal is the signal that is output from the Q-channel mixer 104.

The low IF signal output from the I-channel mixer 102 leads the low IF signal output from the Q-channel mixer 104 by 90 degrees. The two low IF signals each have the same IF frequency, but they are phase shifted by 90 degrees. The low IF signal output from the I-channel mixer 102 is also referred to as an I-channel signal and the low IF signal output from the Q-channel mixer 104 is also referred to as a Q-channel signal. Together, the I-channel signal and the Q-channel signal can be referred to as a complex bandpass signal.

The I-channel mixer 102 is coupled to a first input of an IF filter 106, the first input receives the I-channel signal. The Q-channel mixer 104 is coupled to a second input of the IF filter 106, the second input receives the Q-channel signal. The IF filter 106 is a complex bandpass IF filter which is sensitive to both frequency and phase relationships between the input signals. The IF filter 106 is configured to pass signals where the I-channel signal leads the Q-channel signal by 90 degrees. In an alternative embodiment, the Q-channel mixer 104 generates a phase-quadrature signal which leads the in-phase signal from the I-channel mixer 102 by 90 degrees and the IF filter 106 is configured to pass signals where the I-channel signal lags the Q-channel signal by 90 degrees.

Referring to Figure 2, the output of the IF filter 106 is a phase quadrature pair of signals which are predominately composed of signals with a positive phase sequence. The I-channel

mixer 102 and the Q-channel mixer 104 together form an image reject mixer. The image reject mixer plus the IF limiter 106 produce a quadrature output which is used for the demodulation which will be explained below. Alternatively, a broadband phase shifting means can be used to produce the in-phase and quadrature shifted version of the signals, which are the signals to be used for demodulation as explained below. An additional embodiment includes an image reject mixer which produces a negative phase sequence difference between the I-channel signal and the Q-channel signal. In this case, the image reject mixer is coupled to an IF filter which passes through signals where the I-channel signal lags the Q-channel signal by 90 degrees. The preferred embodiment calls for a superhet receiver that outputs one in-phase signal and one phase-shifted signal. However, additional mixers and filters can be added to the superhet receiver to generate additional phase-shifted output signals.

Referring again to Figure 2, a first output of the IF filter 106 is coupled to an IF limiter 112 via a means of ac coupling 108. The I-channel signal is received by the IF limiter 112. A second output of the IF filter 106 is coupled to an IF limiter 114 via a means of ac coupling 110. The Q-channel signal is received by the IF limiter 114. Both the means of ac coupling 108 and 110 remove any dc components. The IF limiter 112 applies gain and hard limiting action to the I-channel signal whereby the output signal of the IF limiter 112 is a square wave I-channel signal. The rising and falling edges of the square wave correspond to the positive and negative zero crossings of the input I-channel signal to the IF limiter 112. Similarly, the IF limiter 114 applies gain and hard limiting action to the Q-channel signal whereby the output signal of the IF limiter 114 is a square wave Q-channel signal. The rising and falling edges of the square wave correspond to the positive and negative zero crossings of the input Q-channel signal to the IF limiter 114.

The output of each IF limiter 112 and 114 is coupled to a monostable pair. Each monostable pair is comprised of a first monostable coupled in parallel to a serial circuit, the serial circuit includes an inverter and a second monostable. More specifically, a monostable 120 and an inverter 116 are each coupled to the output of IF limiter 112. The inverter 116 is coupled to a

monostable 122. An inverter 118 and a monostable 126 are each coupled to the output of the IF limiter 114. The inverter 118 is coupled to a monostable 124. A monostable is a circuit having only one stable condition, to which it returns in a predetermined time interval after being triggered. Every time the monostable is triggered an output pulse is generated, the output pulse having a specified duration and height. In the preferred embodiment, each monostable has a pulse period equal to one-half the nominal IF frequency. Therefore, at the nominal IF frequency, there is a 50% duty cycle on the monostable. As discussed above, the nominal IF frequency is the same for both the I-channel signal and the Q-channel signal. When the IF frequency is higher than nominal, the duty cycle at the monostable output is greater than 50%. When the IF frequency is lower than nominal the duty cycle at the monostable output is less than 50%. Such a configuration produces a monostable output pulse having a duty cycle proportional to the IF frequency. Combining and filtering the four monostable output pulses improves the recovery of the FM modulation. A data filter low pass filters the train of monostable output pulses to give a mean level. This mean level depends on the duty cycle at the monostable output, which in turn depends on the IF frequency.

The monostable 120 receives the I-channel square wave signal from the IF limiter 112. The monostable 120 is triggered by the rising edge of the I-channel signal to output a pulse. The inverter 116 also receives the I-channel square wave signal from the IF limiter 112. The monostable 122 receives an inverted I-channel signal from the inverter 116. In this case, the monostable 122 is triggered by the rising edge of the inverted I-channel signal, which corresponds to the falling edge of the I-channel signal, and outputs a pulse. The output pulse of the monostable 120 leads the output pulse of the monostable 122 by 180 degrees.

The monostable 126 receives the Q-channel square wave signal from the IF limiter 114. The monostable 126 is triggered by the rising edge of the Q-channel signal to output a pulse. The inverter 118 also receives the Q-channel square wave signal from the IF limiter 114. The monostable 124 receives an inverted Q-channel signal from the inverter 118. The monostable 124 is triggered by the rising edge of the inverted Q-channel signal, which corresponds to the

falling edge of the Q-channel signal, and outputs a pulse. The output pulse of the monostable 126 leads the output pulse of the monostable 124 by 180 degrees. Since the Q-channel lags the I-channel by 90 degrees, the output of the monostable 120 leads the output of the monostable 126 by 90 degrees and the output of the monostable 120 leads the output of the monostable 124 by 270 degrees. The monostables 120, 126, 122 and 124 are triggered respectively by the rising edge in the I-channel signal, the rising edge in the Q-channel signal, the falling edge in the I-channel signal and the falling edge in the Q-channel signal. Hence, there are four output pulses triggered during one cycle of the IF, each 90 degrees apart.

The four output pulses of the monostables 120, 122, 124 and 126 are coupled to a summing circuit 128. The summing circuit 128 combines the pulses and outputs a signal comprising a demodulated signal at a low frequency, approximately 0 to 0.75 MHz, and the carrier signal which is now at four times the IF frequency. The IF carrier signal received by the monostables is cancelled out by the symmetry of the monostables. In other words, the carrier content has been moved from the IF frequency to four times the IF frequency while the data content of the modulated signal remains unchanged. In the preferred configuration as described above, the present invention improves the ability to filter out data from a carrier signal by a factor of four.

The summing circuit 128 is coupled to a data filter 130. The data filter 130 receives the output signal from the summing circuit 128, filters out the spurious frequencies and passes the recovered modulated signal. The spurious frequencies include the carrier signal at four times the IF frequency and random noise.

The data filter 130 is coupled to a data slicer 134 via means for ac coupling 132. The means for ac coupling 132 removes any dc components. The data slicer 134, also known as a comparator or a center slicer, works in a similar way to the IF limiters. The data slicer 134 receives the output signal from the data filter 130 and produces a logic output where the rising and falling edges of the logic output correspond to the positive and negative zero crossings of the data slicer input. The output of the data slicer 134 is approximately the data content of the

original modulated signal. The recovered modulated signal is provided at the output of the data filter 130. There are multiple conventional means for processing this signal. The preferred embodiment utilizes the data slicer 134 but it would be clear to someone skilled in the art that alternative means are available.

The plot in Figure 3 illustrates an example of digital data to be transmitted via a FM radio-frequency signal. This sequence starts with three bits of data '1' followed by four bits of data '0' followed by one bit of data '1' followed by one bit of data '0' followed by one bit of data '1' followed by 2 bits of data '0'. Figures 4-6 illustrate resulting waveforms which are taken at different points within the FM demodulator in response to the input FM radio-frequency signal which carries the digital data illustrated in Figure 3. Figure 4 shows the I-channel signal and the Q-channel signal as they are output from the IF filter 106. During the data '1' the signals in the IF are at a high frequency. When the nominal IF frequency is 1 MHz, the high frequency in this preferred embodiment is approximately 1.5 MHz. During the data '0' the signals are at a much lower frequency. Once again, with a nominal IF frequency of 1 MHz, the low frequency in this example is approximately 0.5 MHz. Figure 5 shows the output of all four monostables, the two I-channel monostables on the upper part of the plot and the two Q-channel monostables on the lower part. Comparing Figure 4 and Figure 5 shows that there is a monostable output pulse for each zero crossing at the outputs of the IF filter 106. Figure 6 shows how the demodulator output is produced from the monostable pulses. The lower trace of Figure 6 shows the analog sum of all the monostable pulses. Although there are many "glitches", the lower trace bears some resemblance to the original modulating data stream. The upper trace of Figure 6 is the demodulator output after low pass filtering in the data filter 130. The FM demodulation has been successfully recovered, and the original data can be regenerated by center slicing the filter output of data filter 130.

As discussed above, a known limitation of the prior art is that the IF frequency must be at least twice the bit rate of the transmission. In the preferred embodiment of the present invention, the multiple pulses per IF cycle lower the minimum IF frequency required to one-half the bit

rate. This allows the present invention to be used with low IF digital FSK receivers where the IF is lower than the bit rate. The preferred embodiment of the present invention utilizes four monostables, thus improving the ability to filter out data from the carrier by a factor of four.

An alternative embodiment includes two monostable configuration which improves the filtering capability by a factor of two. Yet another embodiment utilizes eight monostables which improves the filtering capability by a factor of eight. In this case, the eight monostables are configured into four monostable pairs, each monostable pair receives a corresponding one of the superhet receiver output signals. In order for the superhet receiver to generate the necessary four output signals, as compared to the two output signals of the preferred embodiment, additional mixers and filters can be configured into the receiver to produce two additional phase-shifted output signals. The resulting four output signals are comprised of a first signal, a second signal which lags the first signal by 45 degrees, a third signal which lags the first signal by 90 degrees and a fourth signal which lags the first signal by 135 degrees. The two additional phase-shifted output signals can alternatively be generated by a mathematical means, that is, the use of conventional sum and difference circuitry. The mathematical means can be included within the superhet receiver or coupled externally to the superhet receiver.

The present invention has been described in terms of specific embodiments incorporating details to facilitate the understanding of the principles of construction and operation of the invention. Such reference herein to specific embodiments and details thereof is not intended to limit the scope of the claims appended hereto. It will be apparent to those skilled in the art that modifications may be made in the embodiment chosen for illustration without departing from the spirit and scope of the invention. Specifically, it will be apparent to one of ordinary skill in the art that the device of the present invention could be implemented in several different ways and the apparatus disclosed above is only illustrative of the preferred embodiment of the invention and is in no way a limitation.